EXHIBIT B

BEST AVAILABLE COPY

MOTOROLA

CONFIDENTIAL PROPIETARY

MOTOROLA PATENT COMMITTEE

MOTOROLA INC

[redacted]

AUSTIN INTELLECTUAL PROPERTY DEPARTMENT

Inventor(s) will not fill in

DIVISION NCSG

DISCLOSURE NO. DATE 9/052

COMMITTEE: (INVENTOR MAY SELECT)

- ☐ Circuits/Packaging
- ☐ Process
- ☒ Systems/Software

DISCLOSURE FOR PATENT COMMITTEE

SUBMITTED PURSUANT TO EMPLOYMENT AGREEMENT.

FOR INSTRUCTIONS FOR COMPLETION CONTACT

PATENT COMMITTEE MEMBER IN YOUR ORGANIZATION

1/94 PLEASE SEND TWO (2) COPIES

Inventors must fill in all items 1 to 14. (PLEASE PRINT OR TYPE)
ITEMS 2 TO 4 MAY REQUIRE EXTRA SHEETS. BE SURE THEY ARE SIGNED, WITNESSED AND ATTACHED.

1. Name of the invention. (limit to ten words) .Automatic threshold voltage selection for dual-Vt circuits given high-level designer constraints.
2. What are the problems solved by this invention? see attached sheets
3. Give a complete description of the invention, including its operation, purpose and environment. (Use separate sheets). see attached sheets
4. What improvement over known technology is accomplished by this invention? see attached sheets
5. List the closest known technology (e.g. publication, patent or commercial product) providing the same or similar results: "Design and Optimization of Low Voltage High Performance Dual Threshold CMOS Circuits", Liqiong Wei, et. al. - DAC 98
6. What new elements (e.g. components, circuits, process steps) or combinations of known elements or software algorithm produced the improvement? A new method for generating optimal mixed-Vt circuits based on high-level user constraints.
7. What are the potential applications for use of this invention? Low power, high performance micro processors, micro-controllers and circuit designs.
8. What was the conception date? [redacted] (Attach pertinent log sheets, drawings,etc., to support dates. Always attach the earliest drawing and the earliest written description.) See attached sheets
9. To whom did you first disclose this invention? Name: Gopal Vijayan Date [redacted]
10. When was the device first built and tested? Date? [redacted] Motorola
    State the present location of the device.

DETERMINATION OF LEGAL INVENTORSHIP FOR PATENT APPLICATION MUST BE MADE BY THE INTELLECTUAL PROPERTY DEPARTMENT.

Inventor's signature (IMPORTANT - YOU MUST USE YOUR FULL NAME) - NO INITIALS -

11. Inventors Name: Tim Edwards Signature: [signature] Date: [redacted]

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Page 2 - Disclosure No. _____ **MOTOROLA CONFIDENTIAL PROPRIETARY**

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15. Inventors Name: Chanhee Oh Signature: Chanhee Oh Date: [redacted]
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15b. Inventors Name: Rajendran Panda Signature: [signature] Date: [redacted]
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Dept. No.: RU418 Phone: 512-891-4345 City, State: Austin TX Zip:
Country of Citizenship: India Manager's Name/Mail Drop: David Blaauw F30B

Witness signatures (TWO WITNESSES ARE REQUIRED)
Witness must sign this form and all attachments.
THE WITNESS IN SIGNING THIS FORM ATTEST TO THE FACT THAT THEY UNDERSTAND THE INVENTION.

16. Witness Name: Joe Norton Signature: Joe Norton Date: [redacted]
17. Witness Name: Rajat Chaudhry Signature: [signature] Date: [redacted]

Page 3 - Disclosure No. _____ **MOTOROLA CONFIDENTIAL PROPRIETARY**

Items 18 to 26 are to be filled in by the ENGINEERING MANAGER, LABORATORY MANAGER or above. THE MANAGER IN SIGNING THIS FORM ATTESTS TO THE FACT THAT THE MANAGER UNDERSTANDS THE INVENTION.

18. What product will this invention be used in? (No codes names - use brief description if necessary)
Invention will be used in design of Motorola digital ICs, including the MSIL Quartz

19. When is the estimated shipping date? Not Applicable

20. When (was)(will) the first offer for sale of a product incorporating this invention (be) made?
Date: Not applicable

21. When (was)(will) the first disclosure outside of Motorola (be) made?
How and to whom? State title and date of publication, if any. submission date:

22. What is the market for products incorporating this invention? Microprocessors and microcontroller

23. Who are the potential competitors: Internal CAD organizations within Motorola competitors

24. Did this invention result from work on a development Contract? (YES)(NO) Contract No. No
Who was the contracting party?

25. Discuss the business impact that this invention will have on Motorola. Reduce area, delay and leakage power of Motorola digital ICs.

26. Manager's Name: Bill Read Signature: _____ Date: [redacted]
Phone: 794-4021
Dept. No.: RM532

Witness Signature: _____ Date: [redacted]
Witness Signature: _____ Date: [redacted]

2. Problems Solved

Increasing demand for portable devices has created a greater need for circuits with very low static leakage current. Due to the resulting decrease in supply voltage, power-conscious designers have begun to utilize dual voltage threshold (Vt) transistor designs. In a dual Vt circuit, transistors can have either a high or low threshold voltage characteristic. Low Vt devices have approximately twice the switching speed of a high Vt device, but they contribute a leakage current that is several orders of magnitude higher along with a slightly higher capacitance. In order to meet both the leakage and performance requirements of portable devices, a mixture of low and high Vt devices must be used. In this patent, we propose a new method which automatically select an optimal Vt mixture such that all design constraints are met.

3. Description

This algorithm allows a designer to optimize the Vt mixture based on several constraints, including the maxiumum leakage (Isub) allowance, the minimum performance requirement, and combinations of these two. Other useful constraints are possible and easily integrated. The designer supplies a circuit which is incrementally adjusted until the given constraints are met or until no more adjustment is possible. At each iteration, a transistor (or group of transistors) is chosen for "promotion", or Vt-lowering, based on its promotion sensitivity. This sensitivity is calculated using the projected effect of a Vt change on the timing of the circuit as a whole (via a static timing analysis tool) relative to the increase in circuit leakage (via a fast leakage measurement tool). A promotion affects circuit balance, since the performance characteristic of the promoted transistor changes the balance of critical paths in the circuit. Transistor area is redistributed to compensate, by shifting area from promoted devices to the devices with increased criticality due to the promotion. This redistribution can be done in one of two ways, the first which maintains area while increasing performance, and the second which maintains performance while reducing area. Such a redistibution is easily accomplished using a automated device sizing tool.

Each such iteration (device selection, followed by Vt promotion and area redistribution) moves the circuit incrementally closer to the designer's specified constraints. When all constraints are met (or no more advancement is possible) the process ends, and the resulting solution meets all reachable designer constraints.

4. Improvements Over Known Technology

This algorithm provides a new approach for threshold voltage selection that effectively trades off leakage current, circuit performance, and transistor area. A greedy algorithm based on leakage sensitivity information, this technique results in a solution with excellent characteristics in terms of power, performance AND transistor area.

#91052

Automatic Threshold Voltage Selection for Dual-V_t Circuits

used in the Duet tool

Inventors: Tim Edwards, Abhijit Dharchoudhury, David Blaauw, Supamas Sirichotiyakul, Chanhee Oh, Rajendran Panda

Presentation Overview:

- The Problem
- Prior Art
- The Vt-mix Selection Method
- Application Results
- Competitive Advantages

The Problem

some desirable characteristics for portable devices:

- low leakage current
- high performance

MSIL's Quartz DSP processor will run at 85°C, 0.9V and 100-150Mhz with a maximum leakage current of 50-100uA.

the single-Vt solution

- reducing supply voltage improves power, but hurts performance.
- lowering threshold voltage boosts performance, but hurts leakage

the dual-Vt solution

Designers have begun to use a mixture of high- and low-Vt devices.

- ***high-Vt*: low static leakage, but switch slowly**
- ***low-Vt*: switch quickly, but have very high leakage**

the problem: Which devices should be high and which low?

Prior Art

special structures / techniques

- sleep transistor insertion
- self-biasing
- power-down capability

The top two techniques incur significant area overhead. All three increase design complexity and have restricted application.

manual selection

- can't accurately account for global tradeoffs, suboptimal
- only useful for highly regular topologies (e.g. SRAM)

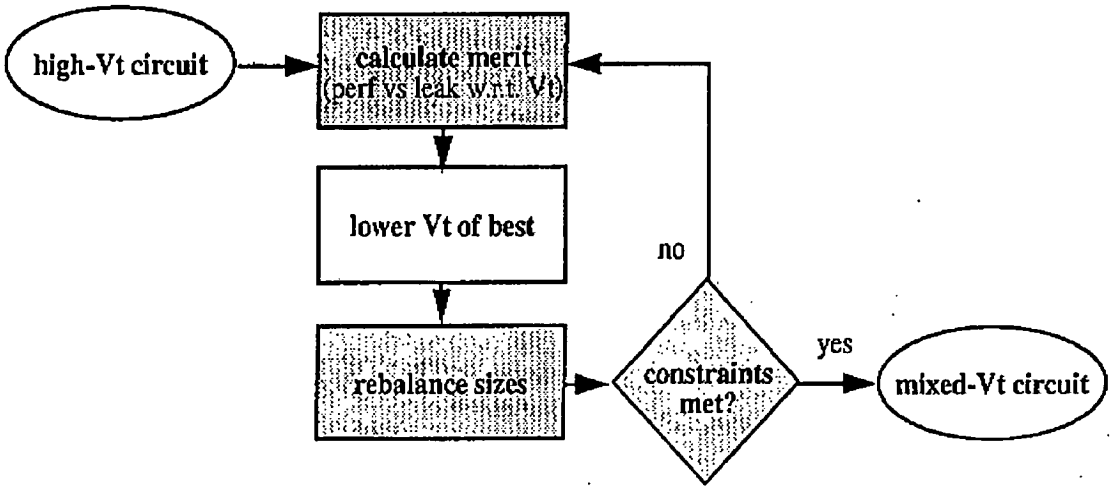
Vt-lowering based on critical path information

- Leakage is unaccounted for (suboptimal power usage)
- Devices remain oversized (suboptimal circuit area)

no other approaches found (in patent searches or publications)

(leakage, current, subthreshold, voltage, dual, optimization, optimize, power)

The Vt-mix Selection Method



unique aspects which can be claimed:

- the overall methodology, accounting for all three key components, leakage, performance, AND area distribution
- the figure of merit, using performance vs. leakage
- the rebalancing step, to redistribute circuit area
- the ability to constrain the solution to meet a leakage budget

Application Results

solution	ckt delay (ns)	improvement vs. all high	leakage (uA)	leakage increase
all high	2.16	-	0.13	-
all low	1.53	29.2%	5.46	42.0x
mixed A	1.72	20.42%	0.62	4.7x
mixed B	1.58	26.85	2.01	15.4x

Competitive Advantages

- This method covers a broad range of possible implementations, and is the only method addressing leakage AND performance.
- We are unaware of any alternatives for achieving results approaching the quality this method yields.
- Motorola is strongly committed to the portable, low-power market.

Products:

- The MSIL Quartz project has begun using this method.

- Both MCORE and Somerset are investigating Dual-Vt processes for their next generation of chips.